Remarks

Applicants respectfully request that this Amendment After Final Action be admitted under 37 C.F.R. § 1.116.

Applicants submit that this Amendment presents claims in better form for consideration on appeal. Furthermore, applicants believe that consideration of this Amendment could lead to favorable action that would remove one or more issues for appeal.

Claims 1, 9-12 and 17-19 have been amended. Claims 5, 6, 8, 13-16, and 21-26 have been canceled. Therefore, claims 1-4, 7, 9-12 and 14 and 17-20 are now presented for examination.

Claims 1-26 stand rejected under 35 U.S.C. §102(b) as being anticipated by Boyd et al. (U.S. Patent No. 5,895,487). Applicant submits that the present claims are patentable over Boyd.

Boyd discloses multiprocessor "node" integrated circuit (IC) having four processors 611 to 614, each with its own L1 cache 621 to 624, respectively. Each of the four L1 caches appear logically to be separate and distinct from each other. Each L1 cache has its own directory which can have, for instance, a four-way set associative, late select organization (or other as determined by performance). In this multiprocessor (MP) configuration, since any block (line) can reside in multiple L1 caches with read permission, an attempt by any one processor to modify such a line will require some coherency mechanism in the other L1 caches. See Boyd at col. 7, ll. 48-63.

Further, the IC includes a cross-point switch 63 with a bus width equal to a cache line width or half-line width is included on-chip. Thus, this remote line can be

transferred from one cache (e.g., L1 cache 623) to L1 cache 621 in one or two cycles. The L1 caches have arrays organized in pseudo-two-port fashion and each L1 array includes four full cache line-width reload and four store back buffers. Such buffers allow a multi-cycle transfer of cache lines from the edge of one cache to the edge of another, and a one cycle read/write from buffer to and from the array. Some compare and priority logic is required to assist the operating system in maintaining the appearance of "in-order execution" of multiple stores on a given cycle. These buffers are used to interface between caches L1 to and from L2 as well as from L1 to and from L1 as described here. In the event that the L1 arrays and logic can eventually be made fast enough, then the above case of a fetching a remote line from L1 cache 623 and storing it in L1 cache 621 would be done directly, on one cycle without need for an intermediate buffer. In this case, these reload and store buffers would be used mainly for multi-cycle transfers to and from L2 and L3 (col. 8, ll. 65 – col. 9, ll. 28).

Claim 1 of the present application recites control logic having a first multiplexer to receive a first cache line from a first dedicated cache and to provide the first cache line to a second dedicated cache and a second multiplexer to receive a second cache line from the second dedicated cache and to provide the second cache line to the first dedicated cache. Applicant submits that Boyd does not disclose such a feature. Instead Boyd discloses a cross-point switch that transfers a line latched into a reload buffer in one cache array to another cache. Nevertheless, such functionality is not equivalent to a first multiplexer to receive a first cache line from a first dedicated cache and to provide the first cache line to a second dedicated cache and a second multiplexer to receive a second

cache line from the second dedicated cache and to provide the second cache line to the first dedicated cache. Thus, claim 1 is patentable over Boyd.

Claims 2-4 and 7 depend from claim 1. Therefore, claims 2-4 and 7 are also patentable over Boyd.

Claim 9 recites control logic having a first fill buffer to receive a first cache line from a first dedicated cache and to provide the first cache line to a second dedicated cache and a second fill buffer to receive a second cache line from the second dedicated cache and to provide the second cache line to the first dedicated cache. Applicant submits that Boyd also fails to disclose this feature. Boyd discloses each L1 cache array having four store back buffers that are used to interface between L1 cache. However, the store back buffers disclosed in Boyd is not equivalent to the write buffers included within control logic as claimed in claim 9. Therefore, claim 9 is patentable over Boyd. Since claims 10 and 11 depend from claim 9, claims 10 and 11 are also patentable over Boyd.

Claim 12 recites transferring a first cache line from a first dedicated cache to a first multiplexer within control logic, transferring the first cache line from the first multiplexer to a second dedicated cache, transferring a second cache line directly from the second dedicated cache to a second multiplexer and transferring the second cache line from the second multiplexer directly to the first dedicated cache. For the reasons described above with respect to claim 1, claim 12 is also patentable over Boyd.

Claim 17 recites transferring a first cache line from a first dedicated cache to a first write buffer within control logic, transferring the first cache line from the first write buffer to a second dedicated cache, transferring a second cache line directly from the second dedicated cache to a second write buffer and transferring the second cache line

from the second write buffer directly to the first dedicated cache. For the reasons described above with respect to claim 9, claim 17 is also patentable over Boyd.

Claim 18 control logic having a first multiplexer to receive a first cache line from a first dedicated cache and to provide the first cache line to a second dedicated cache and a second multiplexer to receive a second cache line from the second dedicated cache and to provide the second cache line to the first dedicated cache. For the reasons described above with respect to claim 1, claim 18 is also patentable over Boyd. Because claims 19 and 20 depend from claim 18, claims 19 and 20 are also patentable over Boyd.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
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